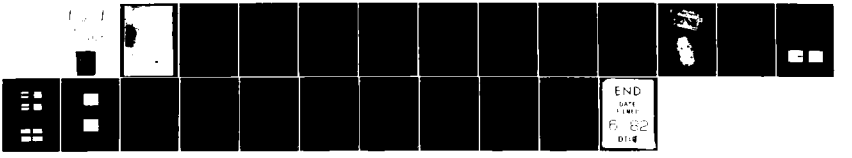
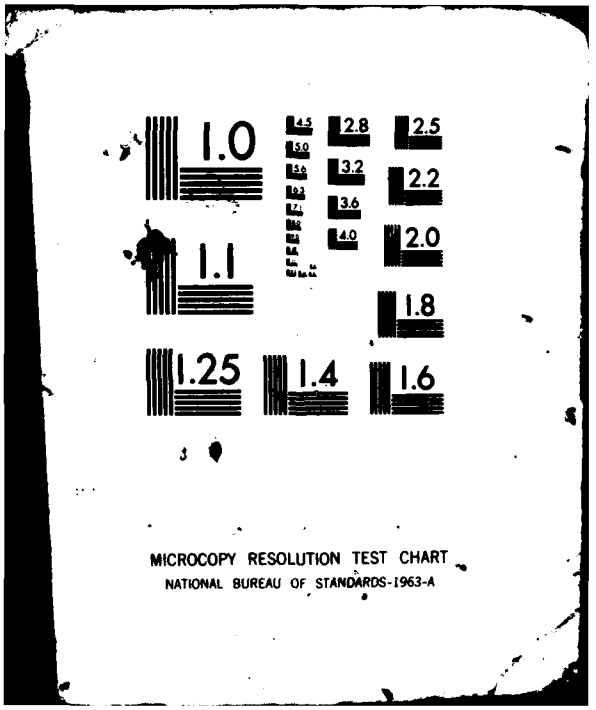
AD-A114 570 ROYAL SIGNALS AND RADAR ESTABLISHMENT MALVERN (ENGLAND) F/G 14/2
HIGH SPEED SAW SPECTRUM ANALYSER DATA HANDLING.(U)
1982 T I BROWNING
UNCLASSIFIED RSRE-MEMO-3450 DRIC-BR-83015 NL




1.0
1.1
1.25
1.4
1.6
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3.2
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4.0
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MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

ROYAL SIGNALS AND RADAR ESTABLISHMENT

Memorandum 3450

Title: HIGH SPEED SAW SPECTRUM ANALYSER DATA HANDLING

Author: T I Browning

Date: February 1982

SUMMARY

The performance of a typical SAW spectrum analyser module is outlined and the problems of handling the data from such a module are discussed. Details of two very high speed custom made LSI shift registers which facilitate data handling are given, as is a comparison of the uses of the two chips. Systems have been constructed to show the use of the chips in storing and displaying the outputs of the spectrum analyser modules. These demonstration circuits are described in detail along with some results of the performance available from these systems.

RSRE MEMORANDUM NO 3450

HIGH SPEED SAW SPECTRUM ANALYSER DATA HANDLING

T I Browning

CONTENTS

LIST OF FIGURE CAPTIONS

INTRODUCTION

This memo outlines methods of 'front end' data handling of the outputs from a SAW Compressive Receiver. Details of how SAW delay lines may be used to make spectrum analysers can be found in the literature[1]. We will only outline some details of the specification of one such Compressive Receiver made at RSRE. It consists of a compact stack of units forming a module with a 250 MHz input bandwidth, the actual input frequency range is determined by the local oscillator unit. Figure 1 shows one of these modules.

1 250 MHz SAW COMPRESSIVE RECEIVER PERFORMANCE

Input sample width	250 ns	
Measurement time	500 ns	
Duty cycle	50%	
Frequency resolution	4 MHz	(unweighted -4 dB)
I/P frequency range	250 MHz	(actual frequencies determined by LO used)
Sidelobe level, present	-13 dB	(unweighted, may be improved by external weighting)
future	< -30 dB	

The detected output from one of these modules therefore gives us up to 64 'cells' (or bits) of data at a clock rate of 256 MHz. Each cell being 4 MHz wide.

We have combined 4 of these modules to make a 1 GHz bandwidth Spectrum analyser[2]. Figure 2 shows a photograph of the unit.

2 DIGITAL INTERFACES AND DATA HANDLING

We have outlined the specification of one of the SAW spectrum analyser units made at RSRE.

These may have very wide bandwidths (as shown) or more modest bandwidths (of a few 10's of MHz) with much greater frequency resolution (> 30 KHz). These being used in radar and communication bands respectively.

Even with what are modest or small bandwidths for SAW devices (few tens of megahertz) conventional circuits may not be able to cope. The data rate of the system is determined by the SAW input bandwidth.

Even if a system has a measurement time of say 40 μs, this represents a resolution of 1/measurement time which is 25 KHz. So with an input bandwidth of say 40 MHz this gives us 1600 resolvable points, to be read out in the 40 μs period.

So even the 'narrowband' SAW based spectrum analysers may need specialized 'front end' processors and the wideband (> 100 MHz) certainly do.

We have therefore had developed under contract two custom built LSI interface circuits, these were designed by Swindon Silicon Systems and fabricated using Plessey's bipolar process 3.

This memo describes the circuits, and demonstrates their use in data handling for a SAW compressive receiver, we also give the advantages and disadvantages of the two circuits.

While showing their use in SAW sub-systems we believe there should be applications in many other areas and therefore give full specification details of the integrated circuits:

A Serial/Serial (fig 3)

This consists of a 64 bit shift register capable of a clock rate of >250 MHz. The data is fed in at this high rate and may then be held then read out at a slower speed ($\leq$ 40 MHz).

B Serial/Parallel (fig 4)

This consists of a 16 bit shift register capable of being clocked at rates 250 MHz. The input data can then be held and latched in a 16 bit parallel output. Serial outputs are also available so these circuits may be cascaded to give any output bit width one may need.

3 DESCRIPTION OF THE DEMONSTRATION UNITS TO GO WITH THE 1 GHz COMPRESSIVE RECEIVER SYSTEM

A Serial to Serial. (fig 5)

This takes the output of one of the four 250 MHz modules. A logic drive board provides the correct timing signals for the comp Rx. The data being read out by a fast clock burst. This clock consists of 64 pulses at a rate of 256 MHz (ie 250 ns the system sample time). The data is then held, then read out of the shift register by a slow clock at 16 MHz. At the end of the slow clock period the register is ready to store another measurement and the cycle repeats.

For demonstration purposes we generated two ramps which were fed to the X and Y inputs of a scope. One was triggered to a sub-multiple of the slow clock pri this represented an integral number of successive measurements. The other being generated during the slow clock readout period, this representing the data output time ie the frequency of the input signals. The data (actually the inverse) was used to brightness modulate the scope when a signal was present. Photographs of input (rf) and 'B scope' display are shown in figure 6. The quantized nature of the output can clearly be seen on the chirp staircase, as the signal goes from one channel to spanning two then on the next etc. In this demonstration the 'Frequency' ramp was reset when the chirp pulse occurred. This is not a 'real time' display. But served to show the usefulness of SAW Comp Rx's in handling multifrequency mixed CW and chirped pulse inputs.

B Serial/Parallel

In this demonstration we take a real time snap shot of the input spectrum, consisting of 2048 successive compressive Rx measurements covering a time slot of 1 ms. As only one S/R is used the output covers only 16 of the possible 64 output 'channels'. Figure 7 shows a block diagram of the buffer store. A expanded version covering all 64 channels would be a fairly simple extension.

A logic drive board provides the appropriate timing signals for a Comp. Rx module, the output data is clocked into the shift register then latched and

'corner turned' onto a parallel form. When a trigger is received (in our case a push button) the system stores 2048 successive measurements and then stops. In our demonstration we then switch over to a read mode which continually reads out the stored information onto a scope, the memories address being fed to a 12 bit DAC providing a 'time' ramp, the parallel data is turned into a serial form and as this is read out another ramp is generated giving us a 'freq ramp', the data (actually the inverse) is used to Z mod the scope. Figure 8 shows the measurement and display system used. Figures 9 and 10 show some of the capabilities of the system.

4 PRO'S AND CONS OF THE TWO METHODS OF DATA HANDLING

Some of these will have become apparent in reading the descriptions of the two demonstrations.

Serial/Serial

If only an occasional look at the environment is needed then a single serial/serial shift register would be ideal. But if more frequent measurements are required then these devices will have to be stacked in parallel form, see figure 11. So when data is being read out of one,the next one can be used to store the next measurement etc. At least five of these would be needed with appropriate RAM and address circuitry, even then the data rate is approximately 34 MHz, fairly fast RAM is still required and RAM capacity may be limited. Figure 12 shows the form of the data in such a stack using 5 shift registers and 1K RAMs. Another problem can then be seen, that is the data is not in a convenient 'order' and either special addressing of the RAMs is needed or data has to be sorted by the data processor.

Serial/Parallel

This approach trades the speed of the logic circuitry against the number of parallel channels used.

If we use four shift registers we have our 64 bit output. Serial data from the SAW Compressive Receiver at a rate of 256 MHz is clocked into the 'corner turning' shift registers and then held. It is then available in parallel form and may be stored at the system remeasurement rate of 2 MHz.

This has advantages over the serial in/serial out system:

1 Main system operating speed is low, as a consequence of which we can:

- a use low power logic, memory etc.
- b these are readily and cheaply available.
- c system design is easier.

2 Each channel output is constantly available, this offers the use of 'hardwired' detection circuitry on any (or all) channels. One could image counting circuitry to detect and then reject CW, or descriminate between pulses of certain lengths etc.

<u>Both Systems</u>:

1 Boards may be stacked together to provide either greater bandwidth cover and/or greater dynamic range.

2 Units may take say every 10th or 100th measurement and store these, expanding the effective time scale (to either serial/parallel board 10 ms or 0.1 sec etc) this may be useful in doing work averaging spectrum coverage over long time scales.

3 Both systems offer the capability of handling multifrequency CW or pulsed signals.

5 USER MEMORY REQUIREMENTS

As any prospective users of a SAW compressive receiver would have differing data handling requirements. A general purpose buffer store has not been constructed. We have decided to build circuits demonstrating some of the capabilities of the custom LSI circuits. It is felt though that a common requirement would be a data latch circuit comprising of 4 of the 16 bit serial in/parallel out shift registers cascaded together to give a 64 bit parallel output that presents the data at up to the full speed of the SAW system ie 64 bits at up to a 2 MHz rate. The user can then decide what data memory or processing requirements he has and match these to the 64 bit parallel output card. This is available and is compatible with the logic drive board.

6 CIRCUIT DESCRIPTIONS

A Logic Drive Board (see fig 15 for a full circuit diagram)

This performs various functions:

a Provides the timing signals needed by the spectrum analyser units.

b It drives one of the fast serial in, slow serial out shift registers to give a readout display.

c It provides the write enable (W.E) signal needed by the buffer store.

a The circuit is controlled by a master clock going at 256 MHz. This is a surface wave delay line oscillator, the SAW line providing the feedback element of an amplifier chain ensuring there is excess gain around the loop. The tuning and matching components ensure the oscillator goes at the peak frequency of the delay line. This signal is level shifted to make it compatible with ECL levels. The signal is counted down to 2 MHz and NOR'd with the delayed 256 MHz clock (to allow for the propagation delays through the counters) this provides the fast clock oscillator burst (FCO) which is used to clock the data processors. The board provides the impulse drive (I.D) and the gate drive (G.D) signals required by the compressive receiver system. It also provides a timing pulse (TPA). Figures 13 and 14 show the relative positions of the different waveforms.

b In this demonstration model, the FCO is fed to the Serial in/out shift register clock input. The output data from the comp Rx is fed to the data input and also to the hold data input (ETI), this ensures that the input sample is held until it has been readout by the slow clock (SLCK). An internal 'flag' signal (HBO) goes high on the next timing pulse (TPA), this edge triggers the slow clock burst circuitry, the slow clock is the counted down master clock, at 16 MHz. The change of HBO provides the display trigger.

The inverted output data drives an open collector driver which gives us a 15 V swing to drive the display oscilloscope Z mod. See figure 6 for a typical output display.

At the end of the slow clock burst a high to low edge from the counter circuitry gives a trigger to a circuit which resets the shift register on the next timing pulse (ED). The cycle repeats with the next sample being held then readout etc.

B Buffer Store and Display System

The system is controlled by three manually operated switches;

a Write/Read

b Stop/Go

c An enable push button switch

The normal operation cycle would be:

Stop/Go to stop and the Write/Read to write, this has reset the system to address zero. The Stop/Go switch is set to go and the enable push button switch is operated. This starts one complete write cycle ie 2048 successive measurements are stored.

The system then awaits for the Write/read switch to be changed and the enable switch to be operated. The system then repetitively reads out the stored information onto a scope display.

a Storing Data

With the system set to Write and Go, pushing the enable switch effectively acts as a time domain trigger sending a pulse from a 74LS121 to a 74LS112 flip-flop which changes state and sets the 11 bit counter chain (used as the memory address generator) from a preset 0 to incrementing by 1 every time it gets a clock pulse. (Provided by the logic drive board TPA once every 500 ns).

The data transceivers (74LS245) are set to high impedance.

The serial output from the compressive receiver is clocked at a rate of 256 MHz, through the 16 bit shift register, the last 16 bits of data being latched in the shift register and presented in a parallel from upon receipt of the inverted TPA.

These 16 parallel outputs are split into two 8-bit bytes and taken to the I/O buses of the 2 Hitachi HM6116P-3, 2K*8bit CMOS RAM, the data being stored in the location determined by the address counters during the inverted WE pulse supplied from the logic drive board. The $\overline{WE}$ pulse being approximately 150 ns long (the access time of the RAM). Address 2047 is detected and resets the counter flip-flop controller.

b Reading Data

With the system changed over to read and the enable switch pushed the system will start to read the stored information out of the RAM. The readout rate per 16 bit sample is now set by a divided TPA, at a rate of $\frac{1}{4}$ MHz (TPX). The address generator feeds a 12 bit DAC which provides the display X i/p ramp.

The data transceivers are now active and present the 16 bit output to the two 8 bit parallel to serial shift registers (74S165's). The parallel loaded data is then read out in a serial fashion at a rate of 8 MHz (set by a 74S124 voltage controlled oscillator). This is counted by two 74LS191 counters which are initially set to zero then count to 17 and are again reset. The counter outputs drive a DAC which gives a voltage corresponding to the data bit being clocked out at any time. This gives the display Y-ramp.

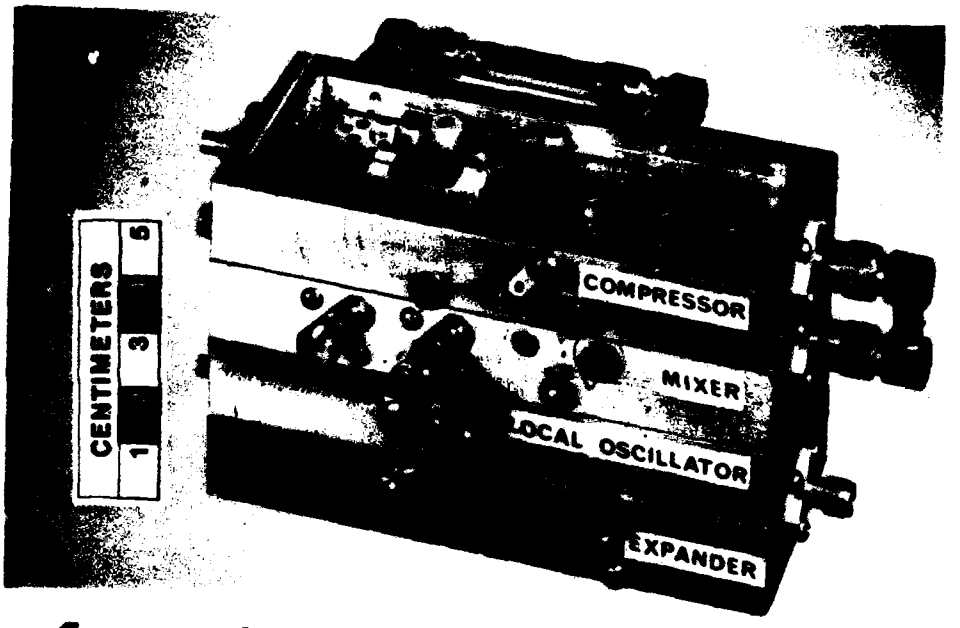
The data is fed through an open collector driver to give the voltage swing required by the Z-mod. input of the display scope.

When address 2047 is detected the address generator is reset to 0 and continues to count until a stop signal or change of mode is received.

REFERENCES

1 Design and application of real-time spectrum-analyser systems
J G Roberts, G L Moule, G Parry IEE Proc Vol 127, PE.F.No 2 April 1980

2 A 1 GHz bandwidth SAW compressive receiver
G L Moule, R A Bale and T I Browning 1981 Ultrasonics symposium.



Compressive Receiver
B = 250 MHz Res = 4 MHz

Fig1

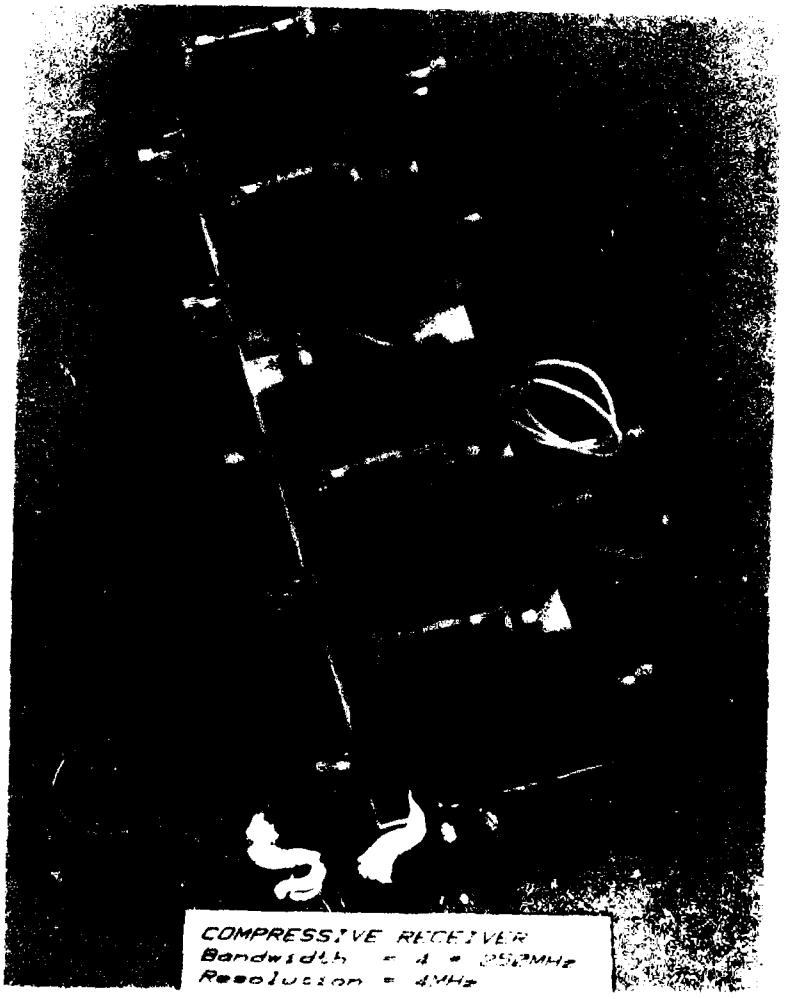
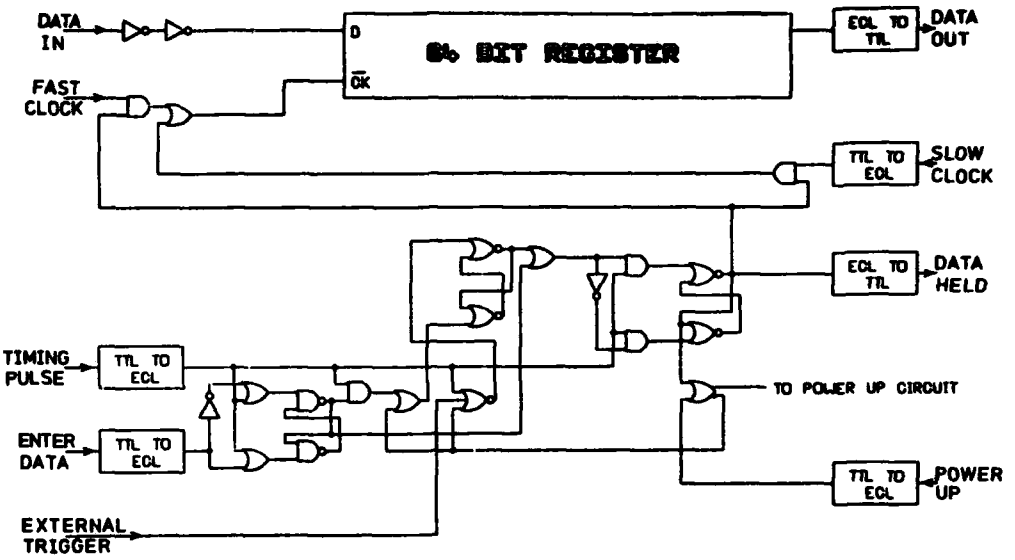
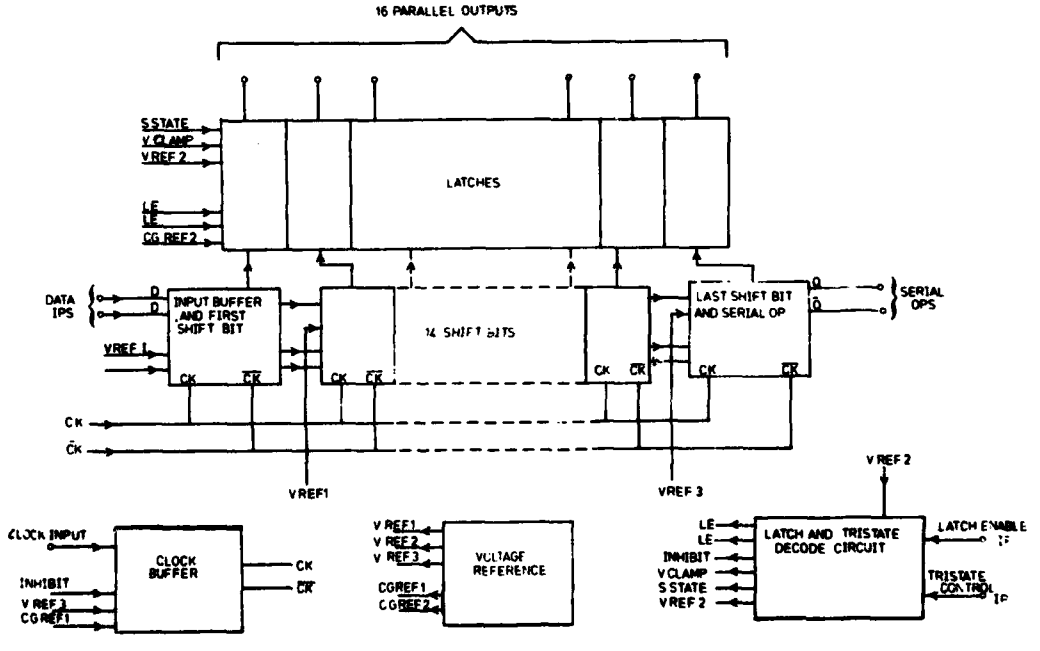


Fig2



SERIAL / SERIAL

Fig 3



SERIAL/PARALLEL

Fig 4

MEASUREMENT SYSTEM. SERIAL IN / SERIAL OUT

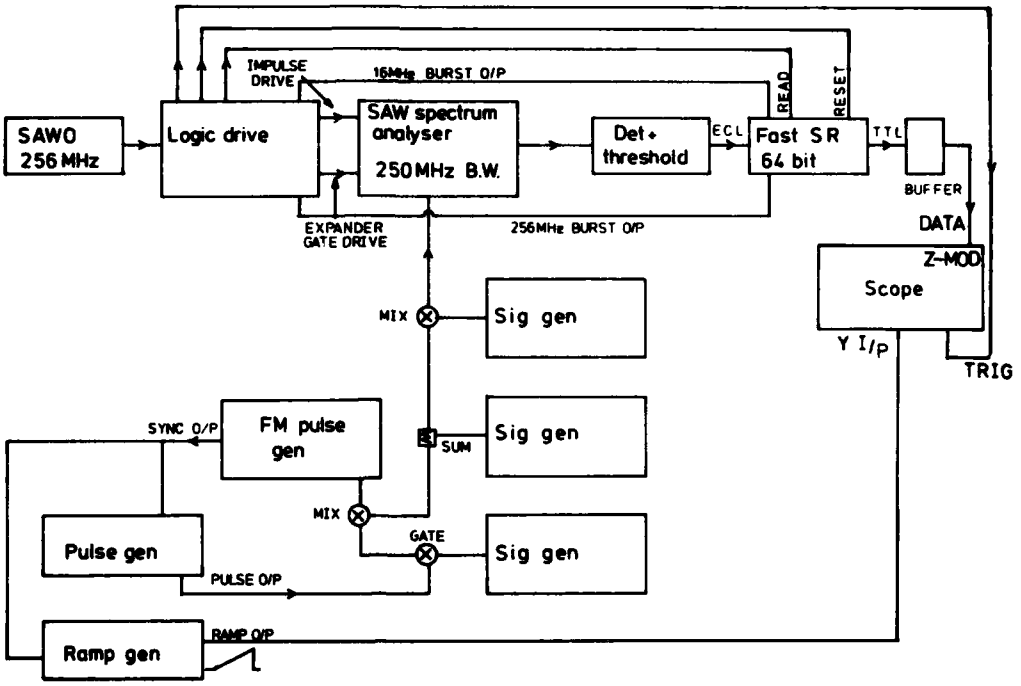


Fig5

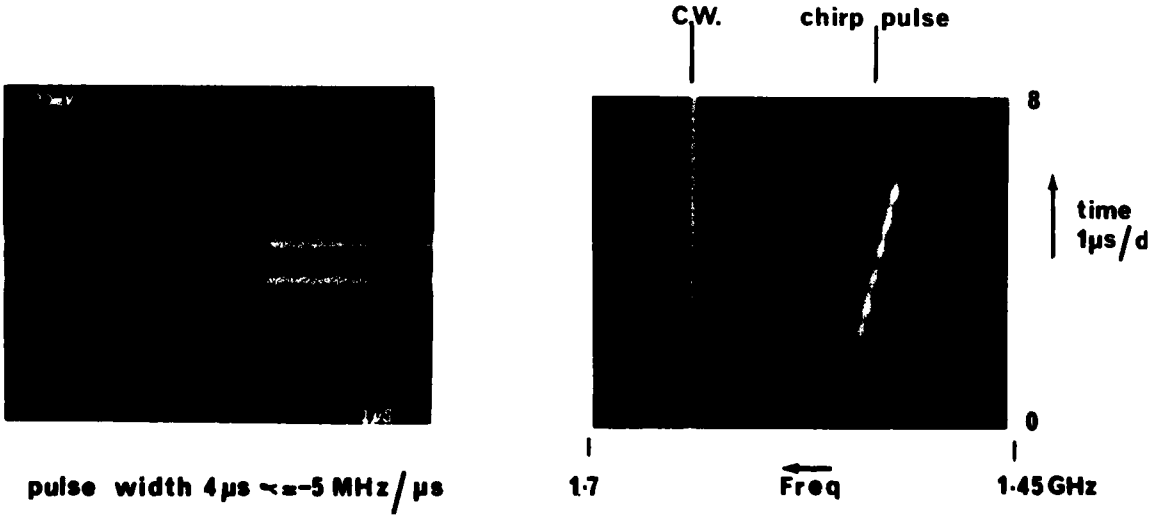
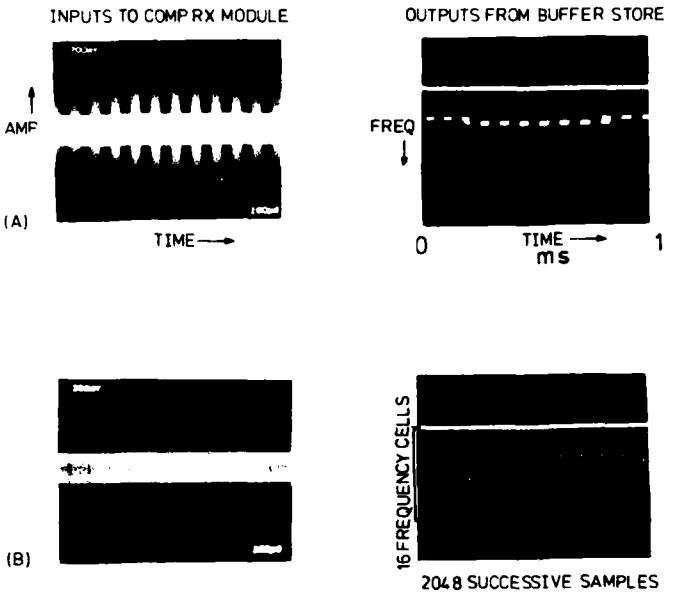


Fig6

COMPRESSIVE RECEIVER BUFFER STORE OUTPUT
(2K*16 BITS)

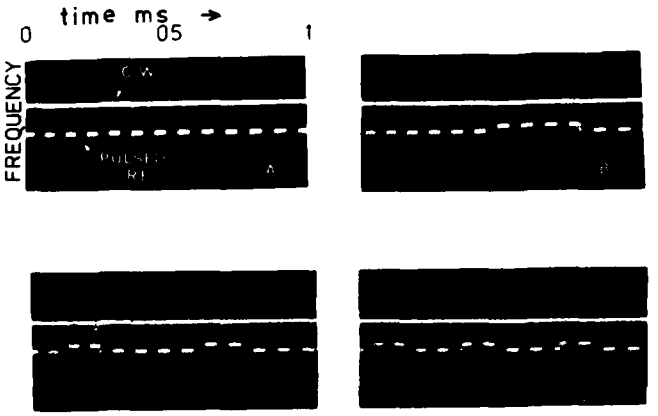


INPUTS CW + FM PULSE PRI 87μs FM DEVIATION = 2 5MHz PK @1KHz RATE
(A) PULSE WIDTH 50μs
(B) PULSE WIDTH 10μs

OUTPUTS CONSISTS OF 2048 SUCCESSIVE COMP RX. SAMPLES STORED IN REAL TIME (2MHz RATE 50% DUTY CYCLE) THEN THE 16 BIT DATA IS REPEATEDLY READOUT AT ¼ MHz RATE

Fig9

COMP RX. BUFFER STORE OUTPUT.

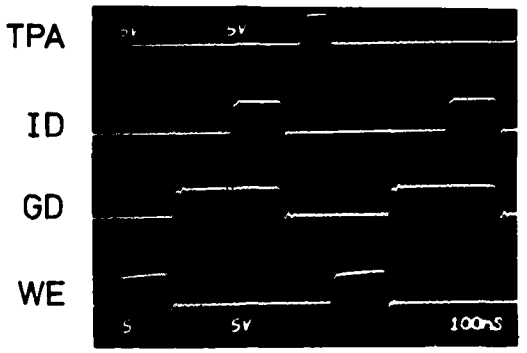


SYSTEM MEASURES FM PULSED RF IN PRESENCE OF CW
PHOTOGRAPHS SHOW RESPONSE TO VARIOUS FM RATES
(AT 2 5MHz pk DEVIATION)

A NO FM B 1KHz C 2KHz D 3KHz

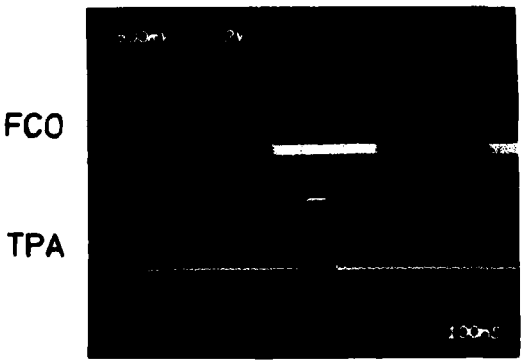
Fig10

Comp. Rx. Logic drive board
output signals



TPA main timing pulse
ID impulse drive
GD gate drive
WE write enable

Fig 13



FCO fast clock oscillator
64cycle burst, 256MHZ rate.

Fig 14

CIRCUIT DIAGRAM OF COMPRESSIVE RECEIVER LOGIC DRIVE.

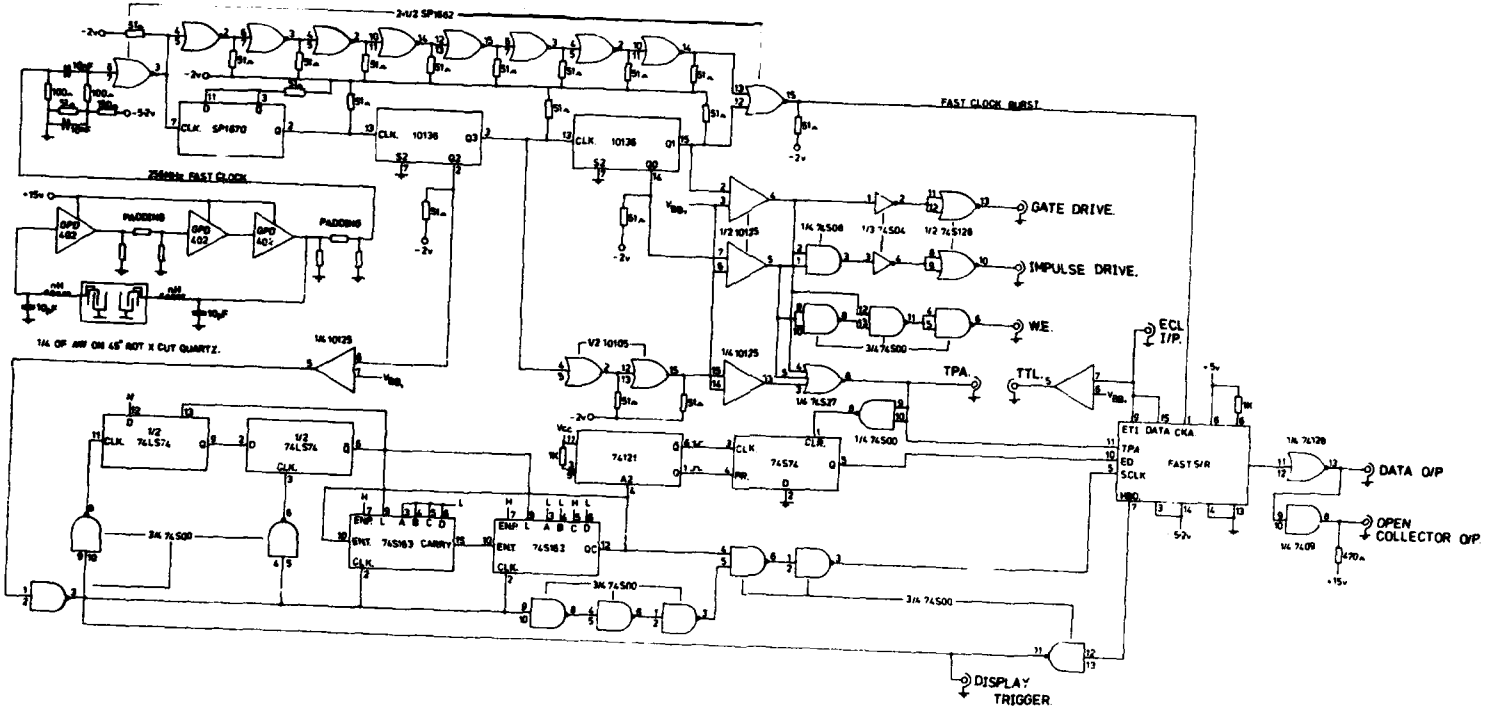


Fig15

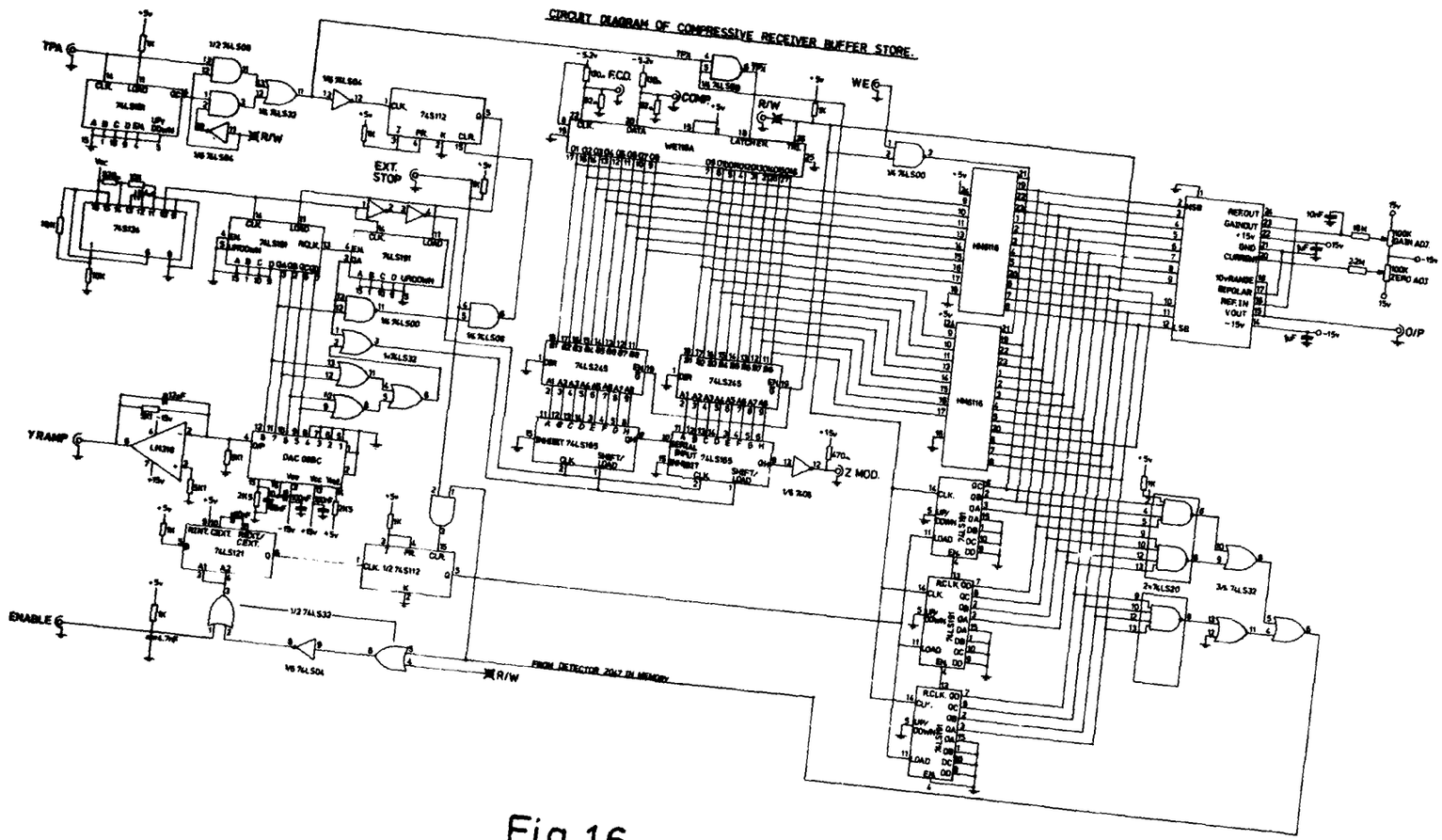

CIRCUIT DIAGRAM OF COMPRESSIVE RECEIVER BUFFER STORE.
TPA
WE
R/W
EXT. STOP
YRAMP
ENABLE
2 MOD.
O/P
FROM DETECTOR 2047 IN MEMORY

Fig 16

SERIAL TO PARALLEL

Swindon Silicon Systems Ltd
Integrated Circuit Design Consultants

10B, Swindon Road
Stratton St. Margaret
Swindon
Wiltshire SN3 4QB
Telephone 0793 825771
Telex 444482 Silcon G

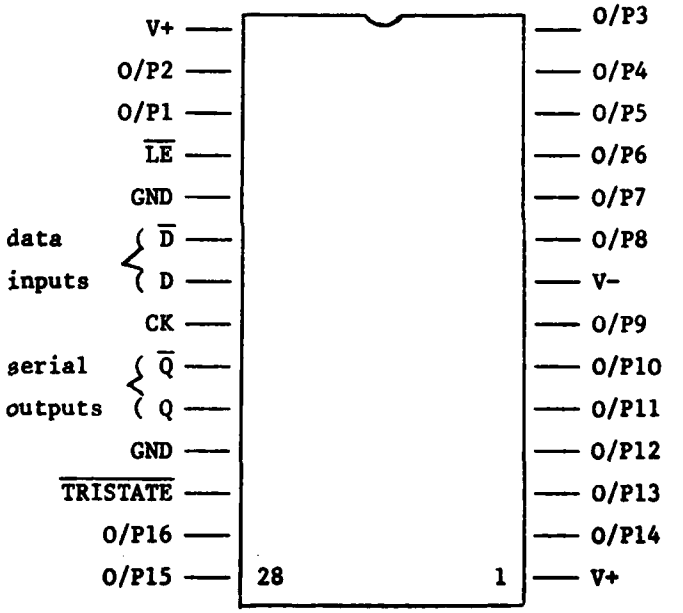
16 BIT HIGH SPEED SHIFT REGISTER

This device is a 16 bit shift register with parallel latched outputs. The shift register operates in the shift right mode, and is capble of operating at shift rates up to 250 MHz. A Schematic diagram of the circuit is shown in fig 2.

FEATURES

* Clock in excess of 250 MHz.
* High speed inputs and outputs ECL 10K compatible
* Cascadable
* Output latch stores
* TTL data outputs
* Tristate

FIG 1. PIN CONNECTIONS



The data inputs, clock and serial data outputs are E.C.L 10K compatible. The data is shifted on the 1 to 0 edge of the clock. The contents of the shift register can be latched out to 16 T.T.L. compatible outputs on the application of a logic '0' to the $\overline{LE}$ input. A logic '0' on the $\overline{LE}$ input also inhibits the clock to prevent a change of data occurring in the shift bits when data is being transferred to the latches. The T.T.L. outputs can be forced into a high impedance state on application of a logic '0' to the $\overline{tristate}$ input. This facility allows the device to be used in bus orientated systems.

The $\overline{LE}$ and tristate bar inputs are T.T.L compatible.

The serial data outputs on the device enable it to be cascaded to produce a 16N bit shift register operating at 250 MHz.

QUICK REFERENCE DATA

PARAMETER	TYPICAL
V+ Supply voltage	+5V
GND Supply voltage	0V
V- Supply voltage	-5.2V
V- Supply current	95 mA
V+ Supply current	17 mA

ELECTRICAL CHARACTERISTICS

1 STATIC CHARACTERISTICS

E.C.L. INPUT LEVELS (CK, D, $\overline{D}$)

T_{AMB} = +25° V- = -5.2V

Minimum input high voltage : V_{EIH} = -0.96V

Maximum input low voltage : V_{EIL} = -1.65V

T.T.L. INPUT LEVELS ($\overline{LE}$, $\overline{TRISTATE}$)

Minimum input high voltage : V_{TIH} = 2.0V

Maximum input low voltage : V_{TIL} = 0.7V

E.C.L. OUTPUT LEVELS (Q, $\overline{Q}$)

Minimum output high voltage : V_{EOH} = -0.96V

Maximum output low voltage : V_{EOL} = -1.65V

T.T.L. OUTPUT LEVELS (O/P 1 to 16)

Minimum output high voltage : V_{OH} = 2.5V

Maximum output low voltage : V_{OL} = 0.5V (sink current = 5mA)

2 DYNAMIC CHARACTERISTICS

PARAMETER	UNITS	MIN	TYP	MAX
Max clock frequency	MHz	250		
Min clock to serial output delay	nsec			2
$\overline{LE}$ to T.T.L. output delay	nsec		25	
T.T.L output rise time	V/nsec		0.3	
T.T.L output fall time	V/Nsec		0.3	

SERIAL/SERIAL 64 BIT

Design Target Specification

Spectrum Analyser Data Readout Integrated Circuit

1 Static Characteristics:

Operating temperature range : $0^{o}C$ to $60^{o}C$ (see note 1)
Supply Voltages : V+ = 5.0 $\pm$ 0.5V
: V- = 5.2 $\pm$ 0.25V
Supply Current : I+ = 7mA type 9mA max
: I- = 167mA typ. 220mA max. (powered up)
: I- = 20mA typ. 30mA max (powered down)

E.C.L input levels (D.CKA/CKB.ETI), Device powered up (see note 1).

T_{amb} = $25^{o}C$ (see note 2), V- = -5.2V

Minimum input high voltate : V_{EIH} = -1.0

Maximum input low voltage : V_{EIL} = -1.5

T.T.L. input levels (TPA/TPB,ED,SLCK,PU)

Minimum input high voltage : V_{TIH} = 2.0V

Maximum input low voltage : V_{TIL} = 0.8V

T.T.L output levels (OP,HBO)

Minimum output high voltage : V_{OH} = 2.5V

Maximum output low voltage : V_{OL} = 0.5V (sink current = 5mA)

2 Dynamic Characteristics:

The following characteristics assume a repetitive clock burst is applied to the CKA/CKB input. This clock consists of 64 clock pulses at a frequency of 256 MHz followed by a logic '0' for a period of 250 nsecs.

Minimum delay from clock burst end to TPA/TPB rising edge : 20 nsec
Minimum delay from TPA/TPB rising edge to clock burst start : 120 nsec
Minimum width TPA/TPB pulse (logic '1') : 20 nsec
Minimum delay from TPA/TPB falling edge to clock burst start: 20 nsec

Dynamic Characteristics (continued)

Maximum slew rate of TPA/TPB pulse	: 200 V/μsec
ED set up and release time (w.r.t TPA/TPB rising edge)	: 10 nsec typ
Minimum delay from TPA/TPB falling edge to ETI falling edge (ETI rising edge may occur during TPA/TPB pulse. Hold will occur on next TPA/TPB pulse)	: 30 nsec
Minimum delay from ETI rising edge to TPA/TPB rising edge	: 20 nsecs
Minimum width of ETI pulse (logic '1')	: 10 nsec
Maximum clock input frequency on SLCK input	: 40 MHz
Maximum clock to output delay (SLCK to OP)	: 25 nsec
Minimum slew rate of SLCK input	: 20 V/μsec

NOTE 1 A package thermal coefficient of 50°C/watt is assumed. To obtain this, a heat sink must be applied (the thermal coefficient of a 16 lead dilmon without an additional heat sink is 100°C/watt)

NOTE 2 The ECL input threshold has a temperature coefficient of 1.3 mV/°C. (input threshold becomes more positive as temperature increases)

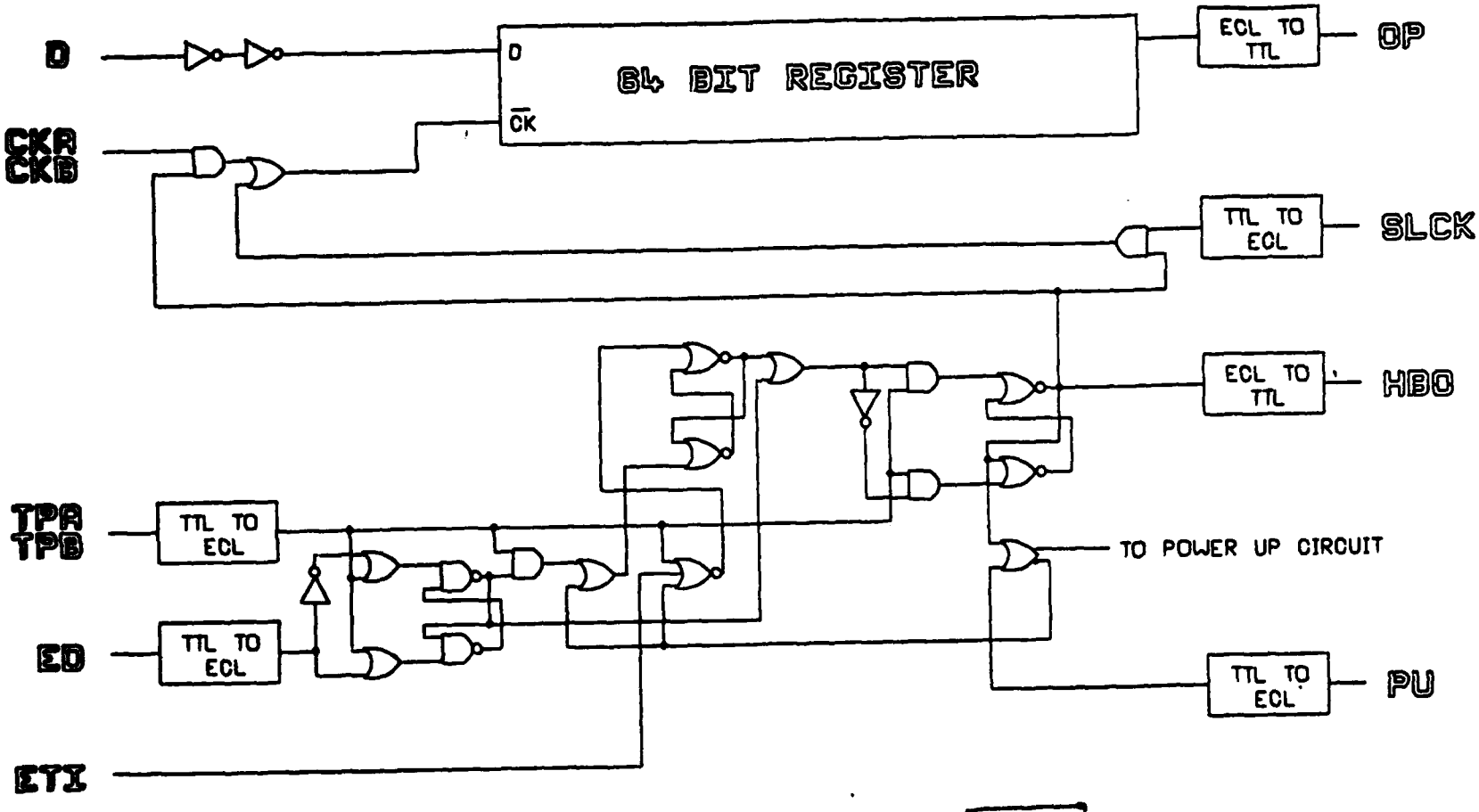


Fig 2

	64 BIT SHIFT REGISTER	DRAWING No		
		ISSUE	1	
		NAME	C.BUNNEY	

END

DATE
FILMED

6 82

DTIC